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DATE MAILED: 01/27/2006

APPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,163		02/17/2004	Roger A. Mock	DP-310331	1265
	7590	01/27/2006	EXAMINER		
STEFAN V	STEFAN V. CHMIELEWSKI WILLIAMS, ALEXANDER O				
DELPHI TEC	CHNOLO	OGIES, INC.			
Legal Staff N	Iail Code	:: CT10C	ART UNIT	PAPER NUMBER	
P.O. Box 900)5		2826		
Kokomo, IN	46904-	9005	DATE MALLED ALIGNOOM		

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.		Applicant(s)	
		10/780,163		MOCK ET AL.	
Office Action St	ımmary	Examiner		Art Unit	
		Alexander O. Wi	lliams	2826	
The MAILING DATE of Period for Reply	this communication app	pears on the cove	r sheet with the c	orrespondence ad	ddress
A SHORTENED STATUTOR WHICHEVER IS LONGER, F - Extensions of time may be available un after SIX (6) MONTHS from the mailing - If NO period for reply is specified above - Failure to reply within the set or extend Any reply received by the Office later th earned patent term adjustment. See 3	ROM THE MAILING D. der the provisions of 37 CFR 1.1 date of this communication. at the maximum statutory period and period for reply will, by statute an three months after the mailing	ATE OF THIS CO 36(a). In no event, how will apply and will expire e, cause the application t	OMMUNICATION ever, may a reply be tim SIX (6) MONTHS from to become ABANDONED	. ely filed the mailing date of this o O (35 U.S.C. § 133).	
Status					
1) Responsive to commur	ication(s) filed on 14 O	october 2005.			
2a) This action is FINAL .		s action is non-fin	al.		
3)☐ Since this application is closed in accordance w		•			e merits is
Disposition of Claims					
4)⊠ Claim(s) <u>1-20</u> is/are per 4a) Of the above claim(s) 5)□ Claim(s) is/are a 6)⊠ Claim(s) <u>1-6</u> is/are reject 7)□ Claim(s) is/are of 8)□ Claim(s) are sub	s) <u>7-20</u> is/are withdrawi llowed. cted. bjected to.	n from considerat			
Application Papers					
9) The specification is obje	·				
10) The drawing(s) filed on	•	•	-		
Applicant may not request		• • •	•	` ,	ED 4 404/4)
Replacement drawing she 11) The oath or declaration	=	· ·			` '
Priority under 35 U.S.C. § 119					
2. Certified copies of3. Copies of the certified	None of: f the priority document f the priority document tified copies of the prior he International Bureau	s have been rece s have been rece rity documents ha u (PCT Rule 17.2	ived. ived in Applications ave been receive (a)).	on No d in this National	Stage
Attachment(s) 1) Notice of References Cited (PTO-8: 2) Notice of Draftsperson's Patent Dra 3) Information Disclosure Statement(s Paper No(s)/Mail Date	wing Review (PTO-948)	5) 🔲	Interview Summary (Paper No(s)/Mail Dai Notice of Informal Pa Other:		O-152)

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Serial Number: 10/780163 Attorney's Docket #: DP-310331

Filing Date: 2/17/2004;

Applicant: Mock et al.

Examiner: Alexander Williams

Applicant's election of group I, claims 1-6 drawn to an integrated circuit package, classified in class 257, subclass 696, filed 11/14/05 to the election with traverse of species III, figures 5A-5G (claims 1 to 20), filed 10/11/05, has been acknowledged.

This application contains claims 7-20 drawn to an invention non-elected without traverse. Note: Applicant's further request that claims 7-20 of Invention II be canceled without prejudice, needs to be done with a proper amendment canceling these claims with a proper amendment.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 6 are rejected under 35 U.S.C. § 102(b) as being anticipated by Rostoker (U.S. Patent # 5,767,570).

- 1. Rostoker (figures 1 to 3c) specifically figure 2a show an integrated circuit package 200, comprising: a first non-conductive substrate 216 having a first inner surface; a second non-conductive substrate 210 having a second inner surface; a die 202 disposed between said first and second inner surfaces, said die having a first thickness; and a leadframe 214,212 including a member having a proximal end and a distal end, said proximal end having a second thickness less than said first thickness, said distal end being disposed between said first and second inner surfaces, said distal end being undulated such that said distal end has an effective thickness greater than said second thickness.
- (3) In general terms, the present invention provides package connections to high I/O semiconductor dies by providing at least a first plurality and a second plurality of bond sites on a substrate or leadframe to which electrical connections may be made. ("Bond sites" are formed by the ends of conductive traces or leads which extend inwardly towards a die-receiving area.) In leadframe-type packages (e.g., TAB) the first plurality and second plurality of bond sites are provided in two planes. In substrate-based packages, the first plurality and

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second plurality of bond sites may be provided either on the same surface of the <u>substrate</u> or on opposite surfaces of the <u>substrate</u>. When bond sites are provided on the same side of the <u>substrate</u>, one of the two <u>pluralities</u> of bond sites extends into a <u>die</u>-receiving area, while the other is spaced away from the die-receiving area.

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- (13) The leadframe backing material 216 may be a tape backing, such as mylar of kapton, similar to materials used in other packages. The double-sided semiconductor die 202 has first conductive bump contacts 206 disposed on a first major surface 202a, and second conductive bump contacts 208 disposed on a second major surface 202b. The leadframe 214 comprises a twotier structure, whereby a first plurality of planar leads 214a extend inwardly in a single plane towards a die-receiving area (described hereinbelow with respect to FIG. 2b), and a second plurality of formed (bent out-of plane) leads 214b are bent downwards (as depicted). Inner ends 215a of the first leads 214a provide contact and mounting points to which the doublesided semiconductor die is connected and mounted via the first bump contacts 206. The planar substrate 210 has conductive traces 212 disposed along one (die-facing) surface thereof. Inner ends 215b of the second leads 214b provide contact and mounting points which are connected and mounted to the inner ends 215b of the traces 212 on the substrate 210, preferably by a re-flow soldering technique. The conductive traces 212 extend inwardly (towards the die) further than the ends of the second leads 214b, and connect to the second conductive bump contacts 208. The second bump contacts are preferably re-flow soldered to the inner ends of the conductive traces 212.
- 2. The package of claim 1, Rostoker show wherein said effective thickness is approximately equal to said first thickness.
- 3. The package of claim 1, Rostoker show wherein said distal end is one of offset formed, squirt formed, corrugated formed, and embossed formed.
- 4. The package of claim 1, Rostoker further comprising: at least one first conductive element attached to said first inner surface and in electrical communication with each of said distal end of said member and said die; and at least one second conductive element attached to said second inner surface and in electrical communication with each of said distal end of said member and said die.

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5. The package of claim 4, Rostoker show wherein said at least one first conductive element comprises at least one first bonded copper element, said at least one second conductive element comprising at least one second bonded copper element.

6. The package of claim 4, Rostoker further comprising: at least one first layer of conductive attachment material disposed between said at least one first conductive element and each of said distal end of said member and said die; and at least one second layer of conductive attachment material disposed between said at least one second conductive element and each of said distal end of said member and said die.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/666-678,734,737,738,778,698,691	1/20/06
Other Documentation: foreign patents and literature in 257/666- 678,734,737,738,778,698,691	1/20/06
Electronic data base(s): U.S. Patents	10/25/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams Primary Examiner Art Unit 2826

AOW 1/20/06